

Simulation of III-V Material Based Steep Slope Tunnel FET for RF Harvester Application

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Abstract

Due to the limitation of Sub-threshold Swing (SS) of 60 mV/dec in CMOS, alternately Tunnel FETs (TFETs) are more attractive in recent years since it has high energy efficiency and better switching performance even at a reduced voltage level. Because it has the benefits of Band to Band Tunneling (BTBT) behavior of operating mechanism and achieved a steep slope characteristic of less than 60 mV/dec. Despite these merits due to the band to band tunneling, the conventional Silicon based TFET is suffered from very low and limited ON-state current due to indirect and large energy gap feature. In the indirect band gap, the conservation of momentum occurs only when the absorption and emission of a photon are required which makes the absorption coefficient lower and limits the flow of electron. To address this problem, in this paper, a Hetero-Junction Tunnel FET (HTFET) devices employing with different lower bandgap materials (InAs/GaSb and InGaAs/InP) are designed by using Silvaco TCAD device simulator. The overall DC and analog/RF performance of HTFET devices are being extracted and investigated suitable for RF energy harvesting applications. The InAs/GaSb HTFET has shown a superior in characteristics by achieving a higher ON-state current of 2.3 mA/ μm at $V_{\text{gs}} = 1\text{V}$, OFF current leakage of 4.18×10^{-11} A/ μm , SS of 22.18 mV/dec and cut-off frequency range from MHz to GHz in operation. Under very low ambient RF level or sub-milliwatt (< 0 dBm) level conditions, the conventional CMOS based rectifier in RF harvester shows very poor performance and probably fails to convert RF signal into DC output voltage. This is due to the SS limitation of 60 mV/dec. Hence, HTFET based RF harvester is proposed and implemented in the circuit level by using the Keysight ADS software. The result indicates that a two-stage Dickson voltage multiplier design using InAs/GaSb HTFET can able to produce a DC output of 1.9 V, 1.6 μA @ 0 to -10 dBm, maximum efficiency of 59 % @ -14 dBm, operating frequency of 850 MHz at 10 k Ω loads with a sensitivity of 0 to -25 dBm.

Keywords: tunnel FET, band to band tunneling (BTBT), sub-threshold Swing (SS), RF harvester

References

- [1] Z. Abbas and M. Olivieri, "Impact of technology scaling on leakage power in nano-scale bulk CMOS digital standard cells," *Microelectronics Journal*, vol. 45, no. 2, pp. 179-195, February 2014.
- [2] N. Collaert, A. Alian, H. Arimura, G. Boccardi, G. Eneman, J. Franco, T. Ivanov, D. Lin, R. Loo, and C. Merckling, "Ultimate nano-electronics: new materials and device concepts for scaling nano-electronics beyond the Si roadmap," *Microelectronic Engineering*, vol. 132, pp. 218-225, January 2015.
- [3] S. Datta, H. Liu, and V. Narayanan, "Tunnel FET technology: a reliability perspective," *Microelectronics Reliability*, vol. 54, no. 5, pp. 861-874, May 2014.
- [4] U. E. Avci, D. H. Morris, and I. A. Young, "Tunnel field-effect transistors: prospects and challenges," *IEEE Journal of the Electron Devices Society*, vol. 3, no. 3, pp. 88-95, 2015.

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- [5] H. Liu, S. Datta, and V. Narayanan, "Steep switching tunnel FET: a promise to extend the energy efficient roadmap for post-CMOS digital and analog/RF applications," International Symposium on Low Power Electronics and Design (ISLPED), 2013 IEEE International Symposium, September 2013, pp. 145-150.
- [6] H. Lu and A. Seabaugh, "Tunnel field-effect transistors: state-of-the-art," IEEE Journal of the Electron Devices Society, vol. 2, no. 4, pp. 44-49, May 2014.
- [7] V. Vijayvargiya, B. Reniwal, P. Singh, and S. Vishvakarma, "Impact of device engineering on analog/RF performances of tunnel field effect transistors," Semiconductor Science and Technology, vol. 32, no. 6, May 2017.
- [8] P. Y. Wang and B. Y. Tsui, "Experimental demonstration of P-channel germanium epitaxial tunnel layer (ETL) tunnel FET with high tunneling current and high on/off ratio," IEEE Electron Device Letters, vol. 36, no. 12, pp. 1264-1266, December 2015.
- [9] S. Kumar, E. Goel, K. Singh, B. Singh, M. Kumar, and S. Jit, "A compact 2-D analytical model for electrical characteristics of double-gate tunnel field-effect transistors with a SiO₂/High- κ stacked gate-oxide structure," IEEE Transactions on Electron Devices, vol. 63, no. 8, pp. 3291-3299, June 2016.
- [10] P. Pandey, R. Vishnoi, and M. J. Kumar, "A full-range dual material gate tunnel field effect transistor drain current model considering both source and drain depletion region band-to-band tunneling," Journal of Computational Electronics, vol. 14, no. 1, pp. 280-287, March 2015.
- [11] J. Z. Huang, Y. Wang, P. Long, Y. Tan, M. Povolotskiy, and G. Klimeck, "High-performance complementary III-V Tunnel FETs with strain engineering," arXiv preprint arXiv:1605.00955, 2016.
- [12] S. Takagi and M. Takenaka, "Ultra-low power MOSFET and tunneling FET technologies using III-V and Ge," 2017 IEEE International Compound Semiconductor Integrated Circuit Symposium (CSICS), December 2017, pp. 1-4.
- [13] A. Beohar, A. P. Shah, N. Yadav, and S. K. Vishvakarma, "Design of 3D cylindrical GAA-TFET based on germanium source with drain underlap for low power applications," 2017 International Electron Devices and Solid-State Circuits (EDSSC), 2017, pp. 1-2.
- [14] S. Glass, C. Schulte-Braucks, L. Kibkalo, U. Breuer, J. Hartmann, D. Buca, S. Mantl, and Q. Zhao, "Examination of a new SiGe/Si heterostructure TFET concept based on vertical tunneling," 2017 Fifth Berkeley Symposium on Energy Efficient Electronic Systems & Steep Transistors Workshop (E3S), October 2017, pp. 1-3.
- [15] E. Lind, E. Memišević, A. W. Dey, and L. E. Wernersson, "III-V heterostructure nanowire tunnel FETs," IEEE Journal of the Electron Devices Society, vol. 3, pp. 96-102, January 2015.
- [16] C. Convertino, C. B. Zota, H. Schmid, A. M. Ionescu, and K. E. Moselund, "III-V heterostructure tunnel field-effect transistor," Journal of Physics: Condensed Matter, vol. 30, no. 26, June 2018.
- [17] J. Mehta, W. Borders, H. Liu, R. Pandey, S. Datta, and L. Lunardi, "III-V tunnel FET model with closed-form analytical solution," IEEE Transactions on Electron Devices, vol. 63, no. 5, pp. 2163-2168, May 2016.
- [18] V. P. H. Hu and C. T. Wang, "Optimization of III-V heterojunction tunnel FET with non-uniform channel thickness for performance enhancement and ambipolar leakage suppression," Japanese Journal of Applied Physics, vol. 57, no. 45, March 2018.
- [19] M. Thewissen, B. Sorée, and W. Magnus, "The miniband alignment Field-Effect Transistor: a superlattice-based steep-slope nanowire FET," arXiv preprint arXiv:1609.09372, 2016.
- [20] Y. Taur, J. Wu, and J. Min, "An analytic model for heterojunction tunnel FETs with exponential barrier," IEEE Transactions on Electron Devices, vol. 62, no. 5, pp. 1399-1404, May 2015.
- [21] I. Silvaco, "ATLAS user's manual," Santa Clara, CA, Ver, vol. 5, 2011.
- [22] A. Chakraborty and A. Sarkar, "Investigation of analog/RF performance of staggered heterojunctions based nanowire tunneling field-effect transistors," Superlattices and Microstructures, vol. 80, pp. 125-135, 2015.
- [23] S. Anand, S. I. Amin, and R. Sarin, "Analog performance investigation of dual electrode based doping-less tunnel FET," Journal of Computational Electronics, vol. 15, pp. 94-103, 2016.
- [24] H. Lu, T. Ytterdal, and A. Seabaugh, "Universal TFET model (Version 1.6.8)," nanoHUB, 2015.
- [25] K. Boucart and A. M. Ionescu, "Double-gate tunnel FET with High- κ gate dielectric," IEEE Transactions on Electron Devices, vol. 54, pp. 1725-1733, 2007.
- [26] S. S. Chouhan, M. Nurmi, and K. Halonen, "Efficiency enhanced voltage multiplier circuit for RF energy harvesting," Microelectronics Journal, vol. 48, pp. 95-102, 2016.
- [27] S. Kim, R. Vyas, J. Bito, K. Niotaki, A. Collado, A. Georgiadis, and M. M. Tentzeris, "Ambient RF energy-harvesting technologies for self-sustainable standalone wireless sensor platforms," Proceedings of the IEEE, vol. 102, no. 11, 2014, pp. 1649-1666.
- [28] J. Wang, Y. Zheng, S. Wang, M. Liu, and H. Liao, "Human body channel energy harvesting scheme with -22.5 dBm sensitivity 25.87% efficiency threshold-compensated rectifier," in Circuits and Systems (ISCAS), 2015 IEEE International Symposium on, 2015, pp. 89-92.
- [29] W. Wang, H. Wong, and Y. Han, "A high-efficiency full-wave CMOS rectifying charge pump for RF energy harvesting applications," Microelectronics Journal, vol. 46, pp. 1447-1452, 2015.

