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A Mathematical Framework for Online Constant Coefficient Multiplication

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Abstract

Single and Multiple constant multiplications are key operations in several digital signal processing algorithms. This paper develops a mathematical framework for a novel adaptation of the parallel shift-and-add multiplication algorithm for online arithmetic. Based on this adaptation, online constant coefficient multipliers for single constant multiplication (SCM) and multiple constant multiplications (MCM) of streaming floating-point inputs are presented. A finite impulse response filter implementation on Xilinx Virtex 6 Field programmable gate array (FPGA) is used as an example to illustrate the merits of these filters. The results of this implementation show that online multipliers reduce resource utilization, online delay and increase clock frequency in comparison to existing designs. Online multiple constant multipliers also show an average reduction of 65% in the number of slice LUTs and 37% in the number of slice registers required when compared to existing digit-serial multiple constant multipliers. Thus, the proposed online arithmetic operators appear to be good alternatives for constant coefficient multiplication.

Keywords: real-time, online arithmetic, digital signal processing, single constant multiplication, multiple constant multiplications, field programmable gate array, floating-point

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