## A Novel Investigation Method for the S<sub>21</sub> Detection Circuit

## Ming-Che Lee\*

Department of Mechanical Engineering, National Taipei University of Technology, Taipei, Taiwan Received 12 May 2020; received in revised form 08 July 2020; accepted 08 September 2020 DOI: https://doi.org/10.46604/ijeti.2020.6262

## Abstract

This research proposes a novel method to investigate the performance of the  $S_{21}$  detection circuit. Aiming at low frequencies or DC, the method serves as an efficient way of verification and enjoys the benefit of low testing costs. The novel investigation method is demonstrated at 50 MHz and verified by the scattering parameters at 11.05 GHz. Based on the investigation, a model of process variations is constructed. The length of the interface paths is estimated by the model to be  $63\mu$ m, which is consistent with the corresponding length of 74.6 $\mu$ m in the layout. For the measured phase and magnitude, the model indicates that the process variations in the device under test cause errors of 18.91% and 1.27%, whereas those in the interface paths lead to errors of 1.83% and 1%. Based on the model, practical recommendations are also proposed to further improve the measurement precision in the future.

Keywords: scattering parameters (S-parameters), vector network analyzer (VNA), device under test (DUT), calibration

## References

- [1] K. Kurokawa, "Power waves and the scattering matrix," IEEE Transactions on Microwave Theory and Techniques, vol. 13, no. 2, pp. 194-202, March 1965.
- [2] D. M. Pozar, Microwave engineering, 3rd ed. NJ: John Wiley & Sons, 2005.
- [3] K. Jayaraman, Q. Khan, B. Chi, W. Beattie, Z. Wang, and P. Chiang, "A self-healing 2.4GHz LNA with on-chip S<sub>11</sub>/S<sub>21</sub> measurement/calibration for in-situ PVT compensation," IEEE Radio Frequency Integrated Circuits Symposium, May 2010, pp. 311-314.
- [4] A. Goyal, M. Swaminathan, and A. Chatterjee, "Self-correcting, self-testing circuits and systems for post-manufacturing yield improvement," IEEE 54th International Midwest Symposium on Circuits and Systems (MWSCAS), August 2011, pp. 1-4.
- [5] Y. R. Wu, Y. K. Hsieh, P. C. Ku, and L. H. Lu, "A built-in gain calibration technique for RF low-noise amplifiers," IEEE 32nd VLSI Test Symposium (VTS), April 2014, pp. 1-6.
- [6] D. C. Howard, P. K. Saha, S. Shankar, T. D. England, A. S. Cardoso, R. M. Diestelhorst, et al., "A SiGe 8–18-GHz receiver with built-in-testing capability for self-healing applications," IEEE Transactions on Microwave Theory and Techniques, vol. 62, no. 10, pp. 2370-2380, October 2014.
- [7] J. Nehring, M. Schutz, M. Dietz, I. Nasr, K. Aufinger, R. Weigel, and D. Kissinger, "Highly integrated 4–32-GHz two-port vector network analyzers for instrumentation and biomedical applications," IEEE Transactions on Microwave Theory and Techniques, vol. 65, no. 1, pp. 229-244, January 2017.
- [8] K. Niitsu, T. Nakanishi, S. Murakami, M. Matsunaga, A. Kobayashi, N. M. Karim, et al., "A 65-nm CMOS fully integrated analysis platform using an on-chip vector network analyzer and a transmission-line-based detection window for analyzing circulating tumor cell and exosome," IEEE Transactions on Biomedical Circuits and Systems, vol. 13, no. 2, pp. 470-479, April 2019.
- [9] B. Philippe and P. Reynaert, "An f-band n-probe standing wave detector for complex reflection coefficient measurements in 40-nm CMOS," IEEE Transactions on Microwave Theory and Techniques, vol. 67, no. 10, pp. 4278-4286, October 2019.

<sup>\*</sup> Corresponding author. E-mail address: aslan\_lee@hotmail.com; che@ntut.edu.tw

2

- [10] K. Staszek, "Investigation on optimum parameters of six-port reflectometers," International Journal of Information and Electronics Engineering, vol. 9, no. 1, pp. 30-33, March 2019.
- [11] M. C. Lee and C. Y. Huang, "An integrated detection circuit for transmission coefficients," IEEE Access, vol. 8, pp. 237-252, 2019.
- [12] B. C. Paul, S. Fujita, M. Okajima, T. H. Lee, H. S. P. Wong, and Y. Nishi, "Impact of a process variation on nanowire and nanotube device performance," IEEE Transactions on Electron Devices, vol. 54, no. 9, pp. 2369-2376, September 2007.
- [13] Y. Lu, L. Shang, H. Zhou, H. Zhu, F. Yang, and X. Zeng, "Statistical reliability analysis under process variation and aging effects," 46th ACM/IEEE Design Automation Conference, 2009, pp. 514-519.
- [14] P. R. Zahira, T. C. Esteban, and C. Victor, "Gate sizing methodology with a novel accurate metric to improve circuit timing performance under process variations," Technologies, vol. 8, no. 2, p. 25, May 2020.
- [15] J. S. Yoon, S. Lee, J. Lee, J. Jeong, H. Yun, and R. H. Baek, "Reduction of process variations for sub-5-nm node fin and nanosheet FETs using novel process scheme," IEEE Transactions on Electron Devices, vol. 67, no. 7, pp. 2732-2737, July 2020.
- [16] J. Kong and J. Y. Hur, "Near-threshold L1 data cache for yield management under process variations," IEEE Access, vol. 8, pp. 18558-18570, 2020.
- [17] P. Miliozzi, K. Kundert, K. Lampaert, P. Good, and M. Chian, "A design system for RFIC: challenges and solutions," Proceedings of the IEEE, vol. 88, no. 10, pp. 1613-1632, October 2000.
- [18] P. Putek, R. Janssen, J. Niehof, E. J. W. Maten, R. Pulch, B. Tasic, and M. Gunther, "Nanoelectronic coupled problem solutions: uncertainty quantification of RFIC interference," Progress in Industrial Mathematics at ECMI 2016, June 2016, pp. 271-279.
- [19] S. Banerjee, A. Chaudhuri, and K. Chakrabarty, "Analysis of the impact of process variations and manufacturing defects on the performance of carbon-nanotube FETs," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 28, no. 6, pp. 1513-1526, June 2020.
- [20] J. W. Bandler and A. E. Salama, "Fault diagnosis of analog circuits," Proceedings of the IEEE, vol. 73, no. 8, pp. 1279-1325, August 1985.
- [21] R. Murji and M. J. Deen, "A scalable meander-line resistor model for silicon RFICs," IEEE Transactions on Electron Devices, vol. 49, no. 1, pp. 187-190, January 2002.
- [22] S. Ellouz, P. Gamand, C. Kelma, B. Vandewiele, and B. Allard, "Combining internal probing with artificial neural networks for optimal RFIC testing," 2006 IEEE International Test Conference, 2006, pp. 1-9.
- [23] K. Huang, N. Kupp, C. Xanthopoulos, J. M. Carulli, and Y. Makris, "Low-cost analog/RF IC testing through combined intra- and inter-die correlation models," IEEE Design & Test, vol. 32, no. 1, pp. 53-60, February 2015.
- [24] N. K. Subramani, J. Couvidat, A. A. Hajjar, J. Nallatamby, R. Sommet, and R. Quere, "Identification of GaN buffer traps in microwave power AlGaN/GaN HEMTs through low frequency s-parameters measurements and TCAD-based physical device simulations," IEEE Journal of the Electron Devices Society, vol. 5, no. 3, pp. 175-181, May 2017.
- [25] J. W. Nilsson and S. A. Riedel, Electric circuits, 5th ed. New York: Addison-Wesley, 1996.
- [26] G. Gonzalez, Microwave transistor amplifiers: analysis and design, 2nd ed. NJ: Prentice Hall, 1997.
- [27] M. Drakaki, A. A. Hatzopoulos, and S. Siskos, "CMOS inductor performance estimation using z- and s-parameters," 2007 IEEE International Symposium on Circuits and Systems, May 2007, pp. 2256-2259.
- [28] B. Gustavsen and H. M. J. D. Silva, "Inclusion of rational models in an electromagnetic transients program: y-parameters, z-parameters, s-parameters, transfer functions," IEEE Transactions on Power Delivery, vol. 28, no. 2, pp. 1164-1174, April 2013.
- [29] A. Chandrakasan, W. J. Bowhill, and F. Fox, Design of high-performance microprocessor circuits, US: John Wiley & Sons Inc, 2000.
- [30] S. Natarajan, M. A. Breuer, and S. K. Gupta, "Process variations and their impact on circuit operation," IEEE International Symp. Defect and Fault Tolerance in VLSI Systems (Cat. No.98EX223), November 1998, pp. 73-81.
- [31] Z. Gong and R. Rashidzadeh, "TSV extracted equivalent circuit model and an on-chip test solution," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 35, no. 4, pp. 679-690, April 2016.
- [32] T. H. Lee, Planar microwave engineering, New York: Cambridge University Press, 2004.
- [33] T. H. Lee, The design of CMOS radio-frequency integrated circuits, 2nd ed. New York: Cambridge University Press, 2004.
- [34] S. J. Leon, Linear algebra with applications, 8th ed. NJ: Prentice Hall, 2010.
- [35] William J. Palm III, Introduction to MATLAB 7 for engineers, International ed. New York: McGraw-Hill, 2005.



Copyright<sup>®</sup> by the authors. Licensee TAETI, Taiwan. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY-NC) license (https://creativecommons.org/licenses/by-nc/4.0/).