# A Circuit-Level Implementation of Voltage-Tuning Scheme for Realizing Optical PAM-4 Using Three-Segment Microring Modulator

Rui Wang*

Department of Computer and Electrical Engineering, University of Idaho, Moscow, USA

Received 18 December 2019; received in revised form 08 January 2020; accepted 24 March 2020

DOI: https://doi.org/10.46604/ijeti.2020.5072

## Abstract

Silicon Photonics, as one of the solutions to satisfy ever-increasing data bandwidth growth, becomes more challenging due to the latest technologies such as Internet of Things (IoT). Higher order pulse amplitude modulation (PAM) schemes is one of the answers to push towards higher data transmission in the presence of bandwidth limited optical devices. In this paper, we have implemented a circuit-level PAM-4 transmitter design based on the voltage-tuning scheme for realizing optical PAM-4 using a three-segment microring modulator. Simulation results based on the extracted layout using TSMC 65nm LP technology and IMEC-ePIXfab SiPhotonics ISIPP50G technology show that our proposed circuit-level transmitter structure is able to achieve PAM-4 data rate of 25-Gb/s with extinction ratio of 9dB and PAM-4 energy efficiency of 0.5pJ/bit. The results also verify that the scheme is able to achieve high tuning flexibility, but the proposed transmitter will consume more power as a result.

**Keywords:** interconnect, optical transmitter, photonics IC, PAM-4 transmitters

## References

[1] A. A. Fuqaha, M. Guizani, M. Mohammadi, and M. Aledhari,"Internet of things: A survey on enabling technologies, protocols, and applications," IEEE Communications Surveys Tutorials, vol. 17, no. 4, pp. 2347-2376, 2015.

[2] Y.Sun, R. Shubochkin, and D. Braganza "Technical feasibility of new 200Gb/s and 400Gb/s links for data centers," 2018 IEEE Optical Interconnects Conference, June 2018, pp. 37-38.

[3] T. Shi, T. I. Su, N. Zhang, C. Y. Hong, and D. Pan,"Silicon photonics platform for 400g data center applications," 2018 Optical Fiber Communications Conference and Exposition, March 2018, pp. 1-3.

[4] R. Soref and J. Larenzo, "All-silicon active and passive guided-wave components for = 1.3 and 1.6 m," IEEE Journal of Quantum Electronics, vol. 22, no. 6, pp. 873-879, June 1986.

[5] J. Wang, and Y. Long, "On-chip silicon photonic signaling and process-ing: a review," Science Bulletin, vol. 63, no. 19, pp. 1267-1310, 2018.

[6] P. Dong, S. Liao, D. Feng, H. Liang, D. Zheng, R. Shafiiha, and A. V. Krishnamoorthy, "Low vpp, ultralow-energy, compact, high-speed silicon electro-optic modulator," Optics Express, vol. 17, no. 25, pp. 22484-22490, December 2009.

[7] J. Van Campenhout, Y. Ban, P. De Heyn, A. Srinivasan, J. De Coster, S. Lardenois, and S. Janssen, "Silicon photonics for 56G NRZ optical interconnects," 2018 Optical Fiber Communications Conference and Exposition, March 2018, pp. 1-3.

[8] S. Moazeni, S. Lin, M. Wade, L. Alloatti, R. J. Ram, M. Popović, and V. Stojanović, "A 40-Gb/s PAM-4 transmitter based on a ring-resonator optical DAC in 45-nm SOI CMOS," IEEE Journal of Solid-State Circuits, vol. 52, no. 12, pp. 3503-3516, December 2017.

[9] R. Wang and V. Saxena, "A cmos photonic optical pam4 transmitter linearized using three-segment ring modulator," 2019 IEEE 62nd International Midwest Symposium on Circuits and Systems, August 2019, pp. 1114-111.

[10] U. Pfeiffer and B. Welch, "Equivalent circuit model extraction of flip-chip ball interconnects based on direct probing techniques," IEEE Microwave and Wireless Components Letters, vol. 15, no. 9, pp. 594-596, September 2005.

* Corresponding author. E-mail address: wang2430@vandals.uidaho.edu

Tel.: +001-585-967-8636

[11] Q. Huang, F. Piazza, P. Orsatti, and T. Ohguro, "The impact of scaling down to deep submicron on CMOS RF circuits," IEEE Journal of Solid- State Circuits, vol. 33, no. 7, pp. 1023-1036, July 1998.
[12] T. Chalvatzis, K. H. Yau, R. A. Aroca, P. Schvan, M. T. Yang, and S. P. Voinigescu, "Low-voltage topologies for 40-Gb/s circuits in nanoscale CMOS," IEEE Journal of Solid-State Circuits, vol. 42, no. 7, pp. 1564-1573, July 2007.
[13] T. O. Dickson, K. H. Yau, T. Chalvatzis, A. M. Mangan, E. Laskin, R. Beerkens, and S. P. Voinigescu, "The invariance of characteristic current densities in nanoscale MOSFETs and its impact on algorithmic design methodologies and design porting of SiGe Bi-CMOS high-speed building blocks," IEEE Journal of Solid-State Circuits, vol. 41, no. 8, pp. 1830-1845, August 2006.
[14] S. Liang, D. H. K. Hoe, and C. A. T. Salama, "BiCMOS DCVSL gate," Electronics Letters, vol. 27, no. 4, pp. 346-347, Febuary 1991.
[15] G. Balamurugan, J. Kennedy, G. Banerjee, J. E. Jaussi, M. Mansuri, F. O'Mahony, and R. Mooney, "A scalable 515 Gbps, 1475 mw low-power I/O transceiver in 65 nm CMOS," IEEE Journal of Solid- State Circuits, vol. 43, no. 4, pp. 1010-1019, April 2008.
[16] F. O'Mahony, M. Mansuri, B. Casper, J. E. Jaussi, and R. Mooney, "A low-jitter PLL and repeaterless clock distribution network for a 20Gb/s link," 2006 Symposium on VLSI Circuits 2006. Digest of Technical Papers, June 2006.
[17] B. Analui, J. F. Buckwalter, and A. Hajimiri, "Data-dependent jitter in serial communications," IEEE Transactions on Microwave Theory and Techniques, vol. 53, no. 11, pp. 3388-3397, November 2005.
[18] H. Li, Z. Xuan, A. Titriku, C. Li, K. Yu, B. Wang, and T. Baehr-Jones, "A 25 gb/s, 4.4 v-swing, ac-coupled ring modulator-based WDM transmitter with wavelength stabilization in 65 nm cmos," IEEE Journal of Solid-State Circuits, vol. 50, no. 12, pp. 3145-3159, December 2015.
[19] R. Wang, J. Shawon, and V. Saxena, "A CMOS photonic PAM-4 electro-optic DAC using coupling based microrings," IEEE Int. Midwest Symposium on Circuits and Systems, 2018.

Copyright© by the authors. Licensee TAETI, Taiwan. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY-NC) license (https://creativecommons.org/licenses/by-nc/4.0/).